Designing the Sine Wave Quiet Converter

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Abstract- A few designers have known about the Resonant Converter described here for many years. This type of Resonant Converter has been built mainly in the range of 200 watts to 2 kilowatts, and has been used as a static inverter. However, it has remained relatively obscure in the general literature. The Quiet Converter was developed at Jet Propulsion Laboratory (JPL), Division 38, to power very sensitive instruments. The Quiet Converter produces a sinusoidal voltage across a parallel resonant tank. The inherent low noise from this converter is how the nickname, Quiet Converter, came about. Programs at Jet Propulsion Laboratory (JPL) that have successfully used the low noise environment of the Quiet Converter are, WF/PC-II, Articulated Fold, Mirror Actuators, (Hubbell Space Telescope), MISR (Earth Orbiting System), Raman, Mars 05 ONC and SIM's, CCD Cameras.

Introduction

The Quiet Converter produces a sinusoidal voltage across a parallel resonant tank. The dc output voltage is obtained after rectification and filtering of the sinusoidal secondary voltage. The regulation is achieved by controlling the duty-cycle to the tuned tank by the switching transistors. A comparison of the standard type of PWM control is shown in Figure 1 and the Quiet Converter with its amplitude modulation (AM), shown in Figure 2. This paper will use cgs units.

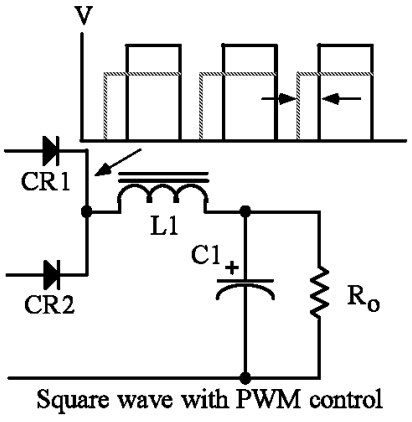

Fig. 1. Standard Type PWM Control.

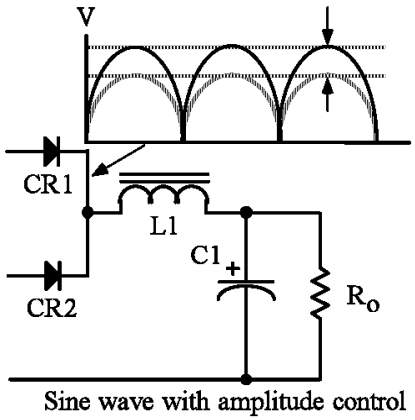

Fig. 2. Quiet Converter with its Amplitude Modulation.

Comparing the Square and Sine wave Converter

The voltage-fed square wave converter circuit is the most widely-used, converter topology. In a voltage-fed converter, the powder source, $V_{in,}$ is connected directly to the transformer through a transistor, Q1, as shown in Figure 3. When the transistor, Q1, is switched on, the full source voltage is applied to the transformer, T1, primary, (1-2). The transistor saturation will be ignored. Conversely, when Q2 is switched on, the full source voltage is applied to the other half of the transformer, T1, primary, (2-3). The primary source voltage, $V_{in,}$ is directly impressed onto the primary of the transformer, T1, and therefore, the voltage across the transformer, T1, is always a square wave.

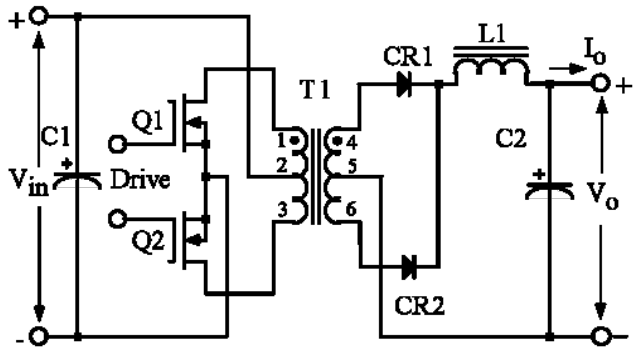

Fig. 3. Typical Square Wave Type Converter.

The main difference between a voltage-fed converter and a current-fed converter is the series inductor, L1 and the tank capacitor, C3, shown in Figure 4. The inductor, L1, is commonly called a feed-choke or series inductor. It has an inductance large enough in value to maintain a continuous current through the circuit under all conditions of line and load. Also, the series inductor, L1, isolates the input dc source from the sine wave voltage across the primary of the transformer, T1. The tank capacitor, C3, tunes the transformer, T1, to the natural operating frequency of the converter.

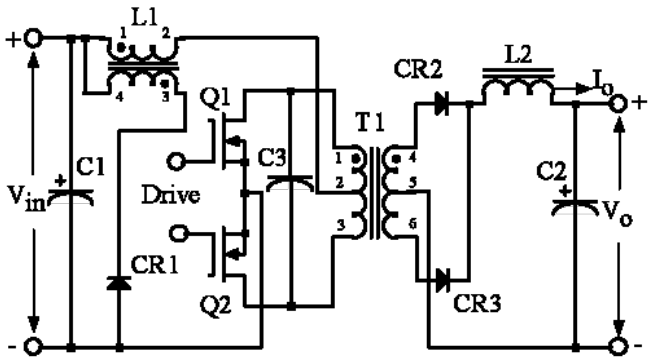

Fig. 4. Paralleled Tuned Sine Wave Converter.

Series Inductor L1

In order to incorporate pulse width modulation (PWM), or a drive circuit that has inherent dead time in which neither transistor is conducting, there must be a means to commutate the current in the series inductor, L1. Adding a winding to the series inductor, L1, is a simple way to commutate the current. When the current flowing in winding, (1-2), is interrupted, the current will now be commutated to the added winding, (3-4).

This procedure is done when connected with proper phasing, through a diode CR1, then, connected back to the dc source to complete the path, as shown in Figure 4. Now, when either transistors, Q1 or Q2, are interrupted, the added winding of the series inductor, L1, commutates the current back into the dc source, thus preventing the destruction of the switching transistors, Q1 and Q2.

Transformer Core Material, T1

The Quiet converter, shown in Figure 4, has changed the operational performance dramatically compared to the square wave converter, shown in Figure 3. The transformer, T1, must have the correct inductance in order to operate correctly. Depending on the design environment the core material can be either a molypermalloy powder core, (MPP), or a ferrite core with a gap. The reason for using a powder core is because it has a built-in gap required for the tank circuit and these cores are available with temperature stabilized permeability. The use of a gap ferrite would perform just as well, but the design must be stable over temperature. The tuning capacitor, C3, should be of high quality with a low ESR and should be stable. The capacitors that were used in the flight power supplies were plastic film, type CRH, to MIL-C-83421.

Quiet Converter Waveforms

The current-fed, sine wave converter waveforms are referenced from Figure 4. The waveforms presented here are copies drawn from an actual photo taken with an oscilloscope camera.

The drain voltage waveform of Q1 is shown in Figure 5. The notches in the waveform, seen in Figure 5, are caused by the dead time or dwell. The converter is properly tuned to the natural frequency.

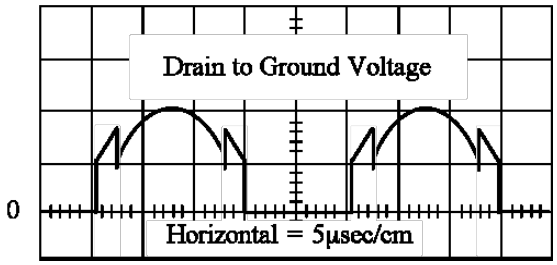

Fig. 5. The Tuning Capacitor C3 is Correct.

The drain voltage waveform of Q1 is shown in Figure 6. The converter is improperly tuned to the natural frequency. The resonant tank capacitor is too small in value.

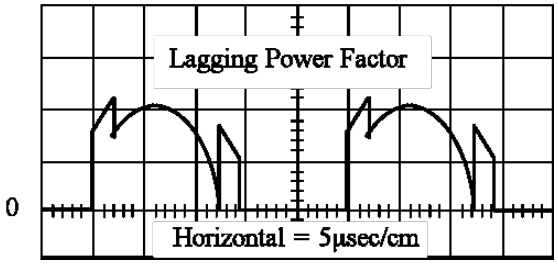

Fig. 6. The Tuning Capacitor C3 is to Small.

The drain voltage waveform of, Q1, is shown in Figure 7. The converter is improperly tuned to the natural frequency. The resonant tank capacitor is too large in value.

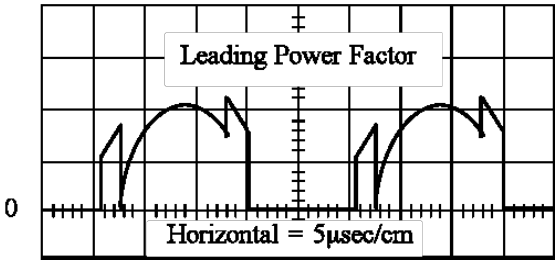

Fig. 7. The Tuning Capacitor C3 is to Large.

The primary voltage waveform is shown in Figure 8, across transformer, T1. The converter is properly tuned to the natural frequency.

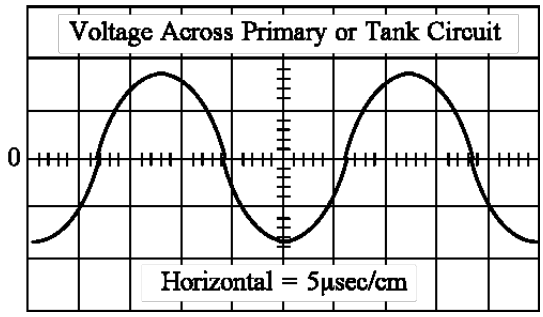

Fig. 8. Voltage Waveform across Transformer, T1.

Commutating diode current waveform is shown in Figure 9. The current is through the series inductor, L1, winding (3-4). The converter is properly tuned to the natural frequency.

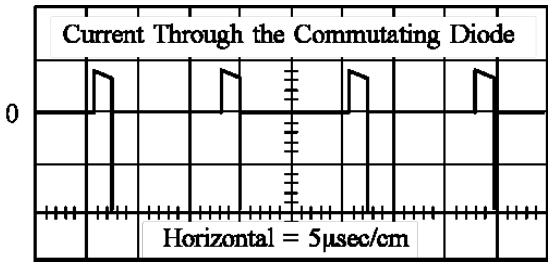

Fig. 9. Current Through the Commutating Diode.

Maximum Transistor on Time, $t_{on(max)}$.

The maximum transistor on time, $t_{on(max)}$, is:
Transistor drive circuits, such as a pulse width modulator (PWM) chip, will have a minimum of dead time, t_d. This dead time or dwell is shown in Figure 10.

$$t_{on(\max)} = \left(\frac{T}{2}\right) - t_d, \quad [\mu\text{sec}] \quad [1]$$

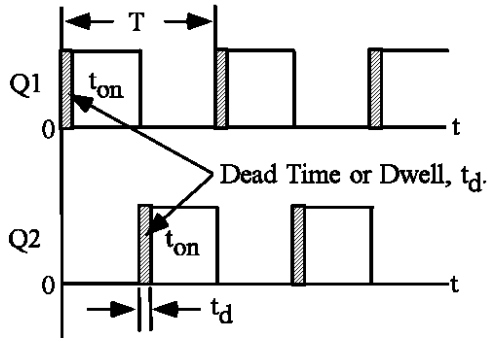

Fig. 10. Base Drive Voltage Dwell Time.

This dwell time, t_d, will have a significant impact the applied ac voltage to transformer, T1. As seen in Figure 5 this dwell time can have a large effect on the applied voltage.

The conversion factor, K_a is:

$$K_a = \frac{\left(4t_{on(\max)} - T\right)}{T\,Sin\left(\frac{t_{on(\max)}180}{T}\right)}, \quad [2]$$

Calculating the Apparent Power, P_t

The apparent power, P_t, is the power associated with the geometry of the transformer. The designer must be able to make allowances for the rms power in each winding. The primary winding handles, P_{in}, the secondaries handle, P_o, to the load. Since the power transformer has to be designed to accommodate the primary power, P_{in}, and the secondary, P_o, then by definition:

$$P_t = P_{in} + P_\Sigma, \quad [\text{watts}]$$
$$P_\Sigma = P_{o1} + P_{o2} + ...P_{on}$$
$$P_{in} = \frac{P_\Sigma}{\eta}, \quad [\text{watts}] \qquad [3]$$
$$P_t = \frac{P_\Sigma}{\eta} + P_\Sigma, \quad [\text{watts}]$$
$$\eta = \text{efficiency}$$

Because of the different winding configurations, the apparent power, P_t, of the transformer will have to be summed to reflect these differences. When the winding has a center tap and produces a discontinuous current, then the power in that winding, whether it is primary or secondary, has to be multiplied by the factor, U, to correct for the rms current in that winding. If the winding has a center tap, then, U = 1.41; if not, then, U = 1. Summing the output power of a multiple-output transformer would be:

$$P_\Sigma = P_{o1}(U) + P_{o2}(U) + ...P_{on}(U), \quad [4]$$

Design Equation Steps for the Quiet Converter

1. The transformer secondary voltage, V_s, is:
V_o = Output voltage
V_d = Diode Drop

$$V_s = (V_o + V_d), \quad [\text{volts}] \quad [5]$$

2. The maximum secondary true power, $P_{s(max)}$, is:

$$P_{s(\max)} = V_s\left(I_{o(\max)}\right), \quad [\text{watts}] \quad [6]$$

3. The minimum secondary true power, $P_{s(min)}$, is:

$$P_{s(\min)} = V_s \left(I_{o(\min)}\right), \quad \text{[watts]} \quad [\ 7\ ]$$

4. The secondary apparent power, P_{sa}, is:
U = 1.41, center tapped winding
U = 1.0, single winding

$$P_{sa} = V_s \left(I_{o(\max)}\right)(U), \quad \text{[watts]} \quad [\ 8\ ]$$

5. If, there is more than one output, then, sum the total secondary maximum apparent load power, $P_{sa\Sigma}$, maximum load power, $P_{ot(max)}$ and minimum load power, $P_{ot(min)}$.

$$P_{sa\Sigma} = P_{sa01} + P_{sa02} + ..., \quad \text{[watts]} \quad [\ 9\ ]$$

$$P_{ot(\max)} = P_{o01(\max)} + P_{o02(\max)} + ..., \quad \text{[watts]} \quad [10\ ]$$

$$P_{ot(\min)} = P_{o01(\min)} + P_{o02(\min)} + ..., \quad \text{[watts]} \quad [\ 11\ ]$$

6. The maximum reflected secondary load resistance, $R_{(max)}$, is:
$R_{(max)}$ = Resistance Value
η = Efficiency

$$R_{(\max)} = \frac{(V_{in})^2(\eta)}{P_{ot(\min)}}, \quad \text{[ohms]} \quad [\ 12\ ]$$

7. The required series inductor inductance, L1, is:
f = fundamental frequency

$$L1 = \frac{\left(R_{(\max)}\right)}{3\omega}, \quad \text{[henrys]} \quad [\ 13\ ]$$

8. The total period, T, is:

$$T = \frac{1}{f}\left(10^6\right), \quad [\mu\text{sec}] \quad [\ 14\ ]$$

9. The maximum transistor on time, $t_{on(max)}$, is:

(See Figure 10.)

$$t_{on(\max)} = \left(\frac{T}{2}\right) - t_d, \quad [\mu\text{sec}] \quad [\ 15\ ]$$

10. The conversion ratio, K_a, is:

$$K_a = \frac{\left(4t_{on(\max)} - T\right)}{T\,Sin\left(\frac{t_{on(\max)}180}{T}\right)}, \quad [\text{factor}] \quad [\ 16\ ]$$

11. The peak voltage, $V_{c(pk)}$, on the resonant capacitor, C3, as shown in Figure 4, is:
K_b = 2, center tapped winding.
K_b = 1, single winding.

$$V_{c(pk)} = \frac{\pi\left(K_a V_{in} K_b\right)}{2}, \quad \text{[volts]} \quad [\ 17\ ]$$

12. The primary rms voltage, $V_{p(rms)}$, is:
K_b = 2, center tapped winding.
K_b = 1, single winding.

$$V_{p(rms)} = \frac{0.707\left(V_{c(pk)}\right)}{K_b}, \quad \text{[volts]} \quad [18\ ]$$

13. The primary maximum reflected secondary current, I_{ps}, is:

$$I_{ps} = \frac{P_{ot(\max)}}{V_{p(rms)}\eta}, \quad \text{[amps]} \quad [\ 19\ ]$$

14. The secondary reflected loads to the primary, R_{SR}, is:
K_b = 2, center tapped winding.
K_b = 1, single winding.

$$R_{SR} = \frac{V_{p(rms)}\left(K_b\right)^2}{I_{ps}}, \quad \text{[ohms]} [\ 20\ ]$$

Note: How the capacitance reactance affects the total percentage of harmonic distortion when:

$$\omega R_{SR} C = 1, \ \approx \ [12\%]$$
$$\omega R_{SR} C = 2, \ \approx \ [\ 6\%]$$
$$\omega R_{SR} C = 3, \ \approx \ [\ 4\%]$$

As a general rule:

$$C_x = \frac{2}{2\pi f\left(R_{SR}\right)}, \quad \text{[farads]}$$

15. Q_T, is a variable that provides the engineer a little latitude with the capacitor value, $(1 < Q_T < 3)$.

$$C_x = \frac{Q_T}{2\pi f\left(R_{SR}\right)}, \quad \text{[farads]} \quad [\ 21\ ]$$

16. The reactance, X_{cx}, of capacitor, C_x, is:
Use a standard capacitor.

$$X_{cx} = \frac{1}{2\pi f C_x}, \quad \text{[ohms]} \quad [\ 22\ ]$$

17. The capacitor rms current, $I_{cx(rms)}$, is:

$$I_{cx(rms)} = \frac{(0.707)(V_{c(pk)})}{X_{cx}}, \quad \text{[amps]} \ [23]$$

18. The total primary current, $I_{tp(rms)}$, is:

$$I_{pt(rms)} = \sqrt{\left(\left(I_{p(rms)}\right)^2 + \left(I_{cx(rms)}\right)^2\right)} \quad \text{[amps]} \ [24]$$

19. The primary tank inductance, L_x, is:

$$L_x = \frac{1}{(2\pi f)^2 C_x}, \quad \text{[henrys]} \ [25]$$

20. The total transformer T1 apparent power, P_t, is:

$$P_t = (\text{Prim VA}) + (\text{Sec VA}) + (\text{Cap VA}), \quad \text{[watts]}$$

$$P_t = \left(\frac{P_{ot(\max)}(U)}{\eta}\right) + (P_{sa\Sigma}) + (K_b V_{p(rms)} I_{cx}), \quad \text{[watts]} \ [26]$$

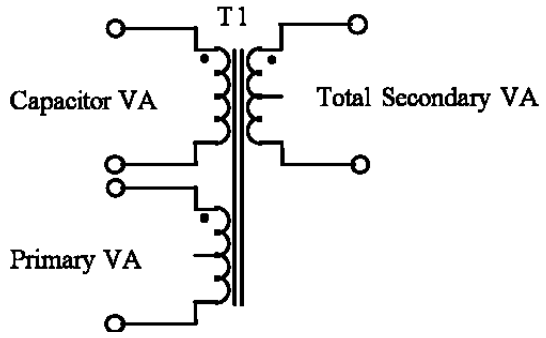

Fig. 11. Total Transformer Apparent Power VA.

21. The core geometry, K_g, is:
K_f is the waveform factor = 4.44
B_{ac} is the operating flux density and its value is an engineering judgment based on the frequency and core material.

$$K_g = \left(\frac{P_t}{0.000029 (K_f)^2 (f)^2 (B_{ac})^2 \alpha}\right), \quad [\text{cm}^5] \ [27]$$

$$K_g = \left(\frac{W_a A_c^2 K_u}{\text{MLT}}\right), \quad [\text{cm}^5] \ [28]$$

Symbols

1. A_c, core iron area in, cm^2
2. α, regulation in, percent %
3. B_{ac}, ac flux in, tesla
4. C_x, performance capacitor in, farads
5. f, frequency in, hertz
6. I_{cx}, capacitor current in, amps
7. I_o, output current in, amps
8. I_{ps}, reflected secondary current in, amps
9. I_{pt}, primary current in, amps
10. J, current density in, amps per cm^2
11. K_a, conversion factor
12. K_e, electrical operating conditions factor
13. K_f, waveform factor = 4.44 sine and 4.0 square
14. K_g, core geometry in, cm^5
15. K_u, window utilization factor
16. K_b, winding correction factor, (see text step 11)
16. L, inductance in, henrys
17. L1, series inductor in, henrys
18. l_g, gap in, cm
19. L_x, primary tank inductance in, henrys
20. MLT, Mean Length turn in, cm
21. η, efficiency in, percent
22. P_o, output power in, watts
23. P_{ot}, total output power in, watts
24. P_s, secondary power in, watts
25. P_{sa}, secondary apparent power in, watts
26. P_Σ, total secondary loss in, watts
27. P_t, apparent power in, watts
28. R, resistance in, ohms
29. R_{SR}, reflected secondary resistance in, ohms
30. T, total period in, usec
31. t_d, dead time in, usec
32. t_{on}, transistor on time in, usec
33. U, multiplication factor (see text step 4)
34. V_c, resonant capacitor voltage in, volts
35. V_d, diode voltage drop in, volts
36. V_{in}, input voltage in, volts
37. V_o, output voltage in, volts
38. V_p, primary voltage in, volts
39. V_s, transformer secondary voltage in, volts
40. VA, volt-amps in, watts
41. W_a, window area in, cm^2
42. X_{cx}, capacitor reactance in, ohms

Acknowledgment

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Reference

[1] McLyman, C., "Transformer and Inductor Design Handbook," 3rd ed., CRC Press, New York, 2004.